Packaging

- New packages have had a major influence on the development of new and next generation products not possible without innovation.
Packaging

- New Packages Impact Design
  - Smaller Footprint
  - Lower Parasitics
  - Lower Height
  - Lower Cost
Package Trends

Figure 3. CPUs have driven the development of high pincount IC packaging. As shown, microprocessors have been packaged in nearly every format over time. (Intel Corp.)
Some Fading Packages

- PLCC & SOJ Packages
- .050” Pitch Gullwing SO & QFP
- MELF’s
- High lead count QFP’s
- 1206 & 1210 Chips
BGA Packages

- Ceramic first developed in 1965 by IBM
- Plastic developed by Motorola 1988
MicroSMT Package

Figure 4. The MicroSMT package in these cutaway views was among the first chip-scale packages fabricated completely on the wafer. (Source: ChipScale Inc.)
Figure 5. Leadless leadframe packages such as the MLF, which is generically a QFN, have become increasingly popular for few-I/O applications. (Amkor Technology Inc.)
Figure 6. Intel's BBUL packaging is bumpless and does not employ solder bumps. (Intel Corp.)
Figure 7. This concept suggests the use of the package to share functions with the IC and accommodate power, ground and cross-chip interconnections. Wafer-level packaging potentially offers more than simple I/O redistribution. (Tessera Inc.)
Figure 8. Chip stacking within a package is a commonly used solution. One highly popular application is the integration of flash memory and SRAM in a single package.
Figure 9. Stacked packaging technologies, such as the μZ Fold-Over and μZ-Ball Stack offer greater functionality in less space than conventional packages. (Tessera)
High Speed Interconnects

Figure 10. The speed bottleneck can be broken by moving high-speed signals to the top surface of IC packages and interconnecting them by means of controlled impedance flexible circuit cables. (SiliconPipe)
Other Expanding Lines

- QFN
- LCN
- LCC
- SOT
- PCN
- BGS/CSP
- Flip Chip
Chip Components

- 0402 Standard
- 0302
- 0201
- 0101
- Buried Resistors
Chip Components

- Standard Fillets
- Minimal Fillets
- Filletless
Chip Components

- Minimal Fillets
Chip Components

- Filletless Lands
Gullwing Leads

- Finer Pitch, narrower leads, shorter foot length, thinner
SON, PowerSOP

- Add heat tabs
PCN, MQFP, L/TQFP Pkg

- Adds thermal pad
- 5-40 mm, 32-304 leads
SOT, SSOT Packages

- Traditional 3-4 Leads
- New Smaller Size 6-8 Leads
LPN, LCN Package (leadless)
LGA Package

![Diagram of LGA Package]
MLF Package (80-100 Lds)
Flip Chip
Wafer Bumping
RF Packages
RF Packages

MARKING (021)

INTERNAL CODE

MONTH INDICATOR 9 (SEPTEMBER)

YEAR INDICATOR 2 (1992)

COMPANY SYMBOL

NEC
RF Packages
LED’s
Land Pattern Trends

- Shorter toe extensions
- Narrower Lands
- Smaller Heel fillets
- Thinner joints
Design Challenges

- More leads per sq in
- More vias required per sq in
- More traces per sq in
- More layers to route
- Thermal Pads
New Design Demands

- Placement is critical
- Optimize Rotations
- Optimize gate and package swaps
- Minimize complex crossovers
- Evaluate package types vs design
PCB Manufacturability

- PC Fab requirements increase
- Smaller vias
- Smaller traces
- More Layers
Assembly

- Higher lead count packages
- Finer pitch increases placement and rotation accuracy
- Thermal Pads complicate repair rework (RR)
- Spacing is tighter making inspection and RR harder
- Lead-Free hi temperatures
Summary

- Evolution is constant change
- Package evolution will continue
- Lots of new high density solutions will appear
- Key is whether they are well thought out to be practical and cost effective in new products